

<b>Notice of References Cited</b>	Application/Control No. 10/617,502	Applicant(s)/Patent Under Reexamination SINGH ET AL.	
	Examiner Leigh Marie Garbowski	Art Unit 2825	Page 1 of 1

#### U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,871,336	03-2005	Anderson, Jason H.	716/9
	B	US-6,779,169	08-2004	Singh et al.	716/16
	C	US-6,631,508	10-2003	Williams, Anthony D.	716/8
	D	US-6,212,668	04-2001	Tse et al.	716/7
	E	US-6,102,964	08-2000	Tse et al.	716/18
	F	US-5,838,584	11-1998	Kazarian, Peter J.	716/16
	G	US-5,521,837	05-1996	Frankle et al.	716/10
	H	US-5,341,308	08-1994	Mendel, David W.	716/7
	I	US-5,224,056	06-1993	Chene et al.	716/7
	J	US-			
	K	US-			
	L	US-			
	M	US-			

#### FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

#### NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	CHOY et al., "incremental Layout Placement Modification Algorithms," IEEE Transactions on CAD of ICs and Systems, Vol. 15, No. 4, April 1996, pages 437-445.
	V	SINGH et al., "Incremental Placement for Layout-Driven Optimizations on FPGAs," IEEE/ACM 2002 Int'l Conference on CAD, pages 752-759.
	W	TOGAWA et al., "An Incremental Placement and Global Routing Algorithm for Field-Programmable Gate Arrays," 1998 IEEE Design Automation Conference, pages 519-526.
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.